QUIZ – ANSWER KEY

QUIZ NO: 102

TOPIC: ELECTRICAL ENGINEERING

DATE: 25/08/2022

1. Which of the following digital logic circuits can be used to add more than 1 – bit simultaneously ?

   [A] Full – adder

   [B] Ripple – carry adder

   [C] Half – adder

   [D] Serial adder

   Answer: B

   Explanation:-

   - A Ripple – carry adder is a parallel binary adder in which the addition of more than 1 – bit data can be done simultaneously. The inputs to a parallel circuit can be sent and processed at once unlike series circuits in which inputs are sent one by one.

2. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?

   [A] Two 2 input AND gates

   [B] Two 3 input AND gates

   [C] Two 2 input OR gates

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[D] Two 3 input OR gates

Answer: A

Explanation:-

Two 2 input AND gates are placed with a NOR – based S – R latch to convert it to an S – R flip – flop. One AND gate is given R in one input and clock in the other. Similarly the second AND gate is given S in one input and clock in the other.

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3. When does a negative level triggered flip-flop in Digital Electronics changes its state ?

   [A] When the clock is negative

   [B] When the clock is positive

   [C] When the inputs are all zero

   [D] When the inputs are all one

   Answer: A

   Explanation:-

   - A negative level triggered flip – flop has a NOT gate present between clock input and the input of AND gate. Thus, the negative level triggered flip – flop change its state when the clock is negative.

4. Which of the following options represent the synchronous control inputs in an S – R flip flop?

   [A] S

   [B] R

   [C] Clock

   [D] Block S and R

   Answer: D

   Explanation:-

   - The input for which the flip flop changes its state when synchronized with the clock is called the synchronous control inputs. For the S – R flip flop, both S and R are synchronous control inputs.

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5. What will be the output from a D flip – flop if the clock is low and D = 0 ?

   [A] 0

   [B] 1

   [C] No Change

   [D] Toggle between 0 and 1

   Answer: C

   Explanation:-

   When the clock is low, the input given to D will have no effect. This is because the set and reset pins of the NAND gates are kept high. When HIGH value is given to NAND gates the output result will be zero.

6. What will be the output from a D flip-flop if D = 1 and the clock is low ?

   [A] No change

   [B] Toggle between 0 and 1

   [C] 0

   [D] 1

   Answer: B

   Explanation:-

   When the clock is low, the input given to D will have no effect. The set and reset pins of the NAND gates are high. When a NAND gate is given 1 as an input to any of the pins, the output will always be 0.

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7. What value is to be considered for a “don’t care condition”?

   [A] 0

   [B] 1

   [C] Either 0 or 1

   [D] Any number except 0 and 1

   Answer: C

   Explanation:-

   A don’t care condition can take 0 or 1 according to the requirement. SOP expressions may consider it to be 1 to increase the number of 1s and POS expressions may consider it to be 0 to increase the number of 0s.

8. What will be the frequency of the output from a JK flip – flop, when J = 1, K = 1, and a clock with pulse waveform is given?

   [A] Half the frequency of clock input

   [B] Equal to the frequency of clock input

   [C] Twice the frequency of clock input

   [D] Independent of the frequency of clock input

   Answer: A

   Explanation:-

   A single flip flop is a divide – by – two device. The frequency of the output from a JK flip – flop, when J = 1, K = 1, and a clock with pulse waveform is given is half the frequency of clock input.

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9. What gate is placed between clock input and the input of AND gate to convert a positive level triggered flip – flop to a negative level triggered flip – flop?

[A] NOR gate
[B] NOT gate
[C] Buffer
[D] NAND gate

Answer: A

Explanation:-

The negative level triggered the flip – flop in Digital Electronics changes its state when the clock is negative. Thus, a negative level triggered flip – flop has a NOT gate present between clock input and the input of AND gate.

10. Which of the following gives the correct number of multiplexers required to build a 32 x 1 multiplexer?

[A] Two 16 x 1 mux
[B] Three 8 x 1 mux
[C] Two 8 x 1 mux
[D] Three 16 x 1 mux

Answer: A

Explanation:-

Two 16 x 1 mux will enable to give 32 inputs. The final output can be obtained after passing the output from each 16 x 1 mux through an OR gate. The select lines will help in selecting a particular output.