QUIZ – ANSWER KEY

QUIZ NO: 145

TOPIC: ELECTRICAL ENGINEERING

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1. The microprocessor of a computer can operate on any information if it is present in _____ only ?

   [A] Program Counter

   [B] Flag

   [C] Main Memory

   [D] Secondary Memory

   Answer: C
   Explanation: If the information isn't in the computer's main store, the microprocessor can't do anything with it. The primary storage area in a computer, also known as main storage or memory, is where data is stored for easy access by the computer's processor. Random-access memory (RAM) and memory are frequently used interchangeably to refer to primary or main storage.

2. Which of the following technology was used by Intel to design its first 8-bit microprocessor?

   [A] NMOS

   [B] HMOS

   [C] PMOS

   [D] TTL

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Answer: C

Explanation: PMOS technology was used for designing the processor because this technology was slow but simple.

3. Which of the following addressing method does the instruction, MOV AX,[BX] represent?

[A] register indirect addressing mode

[B] direct addressing mode

[C] register addressing mode

[D] register relative addressing mode

Answer: A
Explanation:
In register indirect addressing mode the address of the operand is stored in the register. Since the instruction specifies that the register used to refer to the address is accessed indirectly, it represents the register indirect addressing mode.

4. What is the word length of an 8-bit microprocessor?

[A] 8-bits – 64 bits

[B] 4-bits – 32 bits

[C] 8-bits – 16 bits

[D] 8-bits – 32 bits

Answer: A

Explanation: At a time, an 8-bit CPU can process 8 bits of data. Depending on the type of microcomputer, the word length might range from 4 to 64 bits.

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5. In 8-bit microprocessor, how many opcodes are present?

[A] 246

[B] 278

[C] 250

[D] 256

Answer: A

Explanation: In an 8-bit microprocessor, maximum $2^8 = 256$ opcodes are possible. But it consists of only 246 opcodes.

6. Which of the following is not true about the address bus?

[A] It consists of control PIN 21 to 28

[B] It is a bidirectional bus

[C] It is 16 bits in length

[D] Lower address bus lines ($AD_0 – AD_7$) are called "Line number"

Answer: B

Explanation: Data bus in the microprocessor is bidirectional but the address bus is unidirectional. $AD_0 – AD_7$ are the address lines that can be used for both address and data bus lines.

7. Which of the following is true about microprocessors?

[A] It has an internal memory

[B] It has interfacing circuits

[C] It contains ALU, CU, and registers

[D] It uses Harvard architecture

Answer: C

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Explanation: Microprocessors don't have memory and interfacing circuits. They follow Princeton architecture and they contain ALU, CU, and registers inside them.

8. Which of the following is the correct sequence of operations in a microprocessor?

[A] Opcode fetch, memory read, memory write, I/O read, I/O write
[B] Opcode fetch, memory write, memory read, I/O read, I/O write
[C] I/O read, opcode fetch, memory read, memory write, I/O write
[D] I/O read, opcode fetch, memory write, memory read, I/O write

Answer: A

Explanation: Initially, the opcode is fetched from memory, then memory read and write operations are performed followed by I/O read and I/O write operations.

9. The _____ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address ?

[A] GROUP
[B] OFFSET
[C] ORG
[D] LABEL

Answer: C

Explanation: When an ORG is written, the assembler starts the location counter to keep track of the module's allotted address as specified in the directive.
The location counter is initialized to 0000H if the directive is not present.

10. Which of the following is not a property of TRAP interrupt in microprocessor?

[A] It is a non-maskable interrupt
[B] It is of highest priority
[C] It uses edge-triggered signal
[D] It is a vectored interrupt

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Answer: C

Explanation: TRAP interrupt in 8085 microprocessor uses both level and edge-triggered clock because it is of highest priority among all the interrupts.